



In re Application of:

TAE-SUNG KIM

Serial No.:

10/766,564

Examiner:

ERDEM, F.

Filed:

20 January 2004

Art Unit:

2826

For:

NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED IN

A FLAT PANEL DISPLAY

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites and describes the following art references. In accordance with the new regulation set forth in the *Official Gazette Notices:* 05 August 2003 (a copy attached herewith), a copy of the U.S. patent references cited below is not attached.

- U.S. Patent No. 6,180,511 to Kim et al., entitled METHOD FOR FORMING INTERMETAL DIELECTRIC OF SEMICONDUCTOR DEVICE issued on January 30, 2001;
- U.S. Patent Application No. 2002/0085157 to Tanaka et al., entitled ACTIVE
 MATRIX ADDRESSING LIQUID-CRYSTAL DISPLAY DEVICE, published on July
 4, 2002;
- 3. U.S. Patent No. 6,674,502 to Terakado et al., entitled LIQUID CRYSTAL DISPLAY

WITH NITRIDED INSULATING SUBSTRATE FOR TFT, issued on January 6, 2004;

- 4. U.S. Patent No. 6,642,093 to Kubo *et al.*, entitled *METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE*, issued on November 4, 2003;
- U.S. Patent No. 6,608,353 to Miyazaki et al., entitled THIN FILM TRANSISTOR
 HAVING PIXEL ELECTRODE CONNECTED TO A LAMINATE STRUCTURE,
 issued on August 19, 2003;
- 6. U.S. Patent No. 6,534,393 to Zhou et al., entitled METHOD FOR FABRICATING LOCAL METAL INTERCONNECTIONS WITH LOW CONTACT RESISTANCE AND GATE ELECTRODES WITH IMPROVED ELECTRICAL CONDUCTIVITY, issued on March 18, 2003;
- 7. U.S. Patent No. 6,518,630 to You et al., entitled THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY AND METHOD FOR FABRICATING SAME, issued on February 11, 2003;
- 8. U.S. Patent No. 6,410,986 to Merchant *et al.*, entitled *MULTI-LAYERED TITANIUM NITRIDE BARRIER STRUCTURE*, issued on June 25, 2002;
- 9. U.S. Patent No. 6,380,625 to Pramanick *et al.*, entitled *SEMICONDUCTOR INTERCONNECT BARRIER AND MANUFACTURING METHOD THEREOF*, issued on April 30, 2002;
- U.S. Patent No. 6,365,927 to Cuchiaro et al., entitled FERROELECTRIC INTEGRATED CIRCUIT HAVING HYDROGEN BARRIER LAYER, issued on April 2, 2002;

- 11. U.S. Patent No. 6,309,965 to Matshitsch et al., entitled METHOD OF PRODUCING A SEMICONDUCTOR BODY WITH METALLIZATION ON THE BACK SIDE THAT INCLUDES A TITANIUM NITRIDE LAYER TO REDUCE WARPING, issued on October 30, 2001;
- 12. U.S. Patent No. 6,224,942 to Leiphart, entitled *METHOD OF FORMING AN ALUMINUM COMPRISING LINE HAVING A TITANIUM NITRIDE COMPRISING LAYER THEREON*, issued on May 1, 2001;
- 13. U.S. Patent No. 6,096,572 to Nakamura, entitled MANUFACTURING METHOD AND SEMICONDUCTOR DEVICE WITH LOW CONTACT RESISTANCE BETWEEN TRANSPARENT ELECTRODE AND PAD ELECTRODE, issued on August 1, 2000;
- 14. U.S. Patent No. 5,759,916 to Hsu *et al.*, entitled *METHOD FOR FORMING A VOID-FREE TITANIUM NITRIDE ANTI-REFLECTIVE COATING (ARC) LAYER UPON AN ALUMINUM CONTAINING CONDUCTOR LAYER*, issued on June 2, 1998;
- 15. U.S. Patent No. 5,341,026 to Harada et al., entitled SEMICONDUCTOR DEVICE HAVING A TITANIUM AND A TITANIUM COMPOUND MULTILAYER INTERCONNECTION STRUCTURE, issued on August 23, 1994;
- 16. U.S. Patent No. 4,976,839 to Inoue, entitled METHOD OF FORMING A BARRIER LAYER BETWEEN A SILICON SUBSTRATE AND AN ALUMINUM ELECTRODE OF A SEMICONDUCTOR DEVICE, issued on December 11, 1990;

- 17. U.S. Patent No. 4,933,296 to Parks *et al.*, entitled N⁺ AMORPHOUS SILICON THIN FILM TRANSISTORS FOR MATRIX ADDRESSED LIQUID CRYSTAL DISPLAYS, issued on June 12, 1990;
- 18. U.S. Patent No. 4,910,580 to Kuecher *et al.*, entitled *METHOD FOR MANUFACTURING A LOW-IMPEDANCE*, *PLANAR METALLIZATION COMPOSED OF ALUMINUM OR OF AN ALUMINUM ALLOY*, issued on March 20, 1990;
- 19. U.S. Patent No. 4,778,258 to Parks et al., entitled PROTECTIVE TAB STRUCTURE

 FOR USE IN THE FABRICATION OF MATRIX ADDRESSED THIN FILM

 TRANSISTOR LIQUID CRYSTAL DISPLAYS, issued on October 18, 1998;
- 20. U.S. Patent No. 4,646,424 to Parks *et al.*, entitled *DEPOSITION AND HARDENING*OF TITANIUM GATE ELECTRODE MATERIAL FOR USE IN INVERTED THIN

 IFILM FIELD EFFECT TRANSISTORS, issued on March 3, 1987; and
- 21. U.S. Patent No. 4,511,756 to Moeller *et al.*, entitled *AMORPHOUS SILICON SOLAR*CELLS AND A METHOD OF PRODUCING THE SAME, issued on April 16, 1985.
- 22. PCT Publication No. WO 99/08322 to Laska et al., entitled SEMICONDUCTOR WITH METAL COATING ON ITS REAR SURFACES, published on 18 February 1999;
- Japanese Patent Publication No. 09-213656 to Ishida, entitled SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING IT, published on August 15, 1997;

- 24. Japanese Patent Publication No. 04-265757 to Kawasaki, entitled *THIN FILM TYPE THERMAL HEAD*, published on September 21, 1992;
- 25. Japanese Patent Publication No. 64-19763 to Shankar et al., entitled IMPROVED INTEGRATED CIRCUIT STRUCTURE AND ITS FORMATION, published on January 23, 1989;
- 26. Japanese Patent Publication No. 59-232464 to Morimitsu *et al.*, entitled *COMPOUND SEMICONDUCTOR DEVICE*, published on December 27, 1984;
- 27. Japanese Patent Publication No. 62-221159 to Yanai *et al.*, entitled *FORMATION*OF THIN FILM TRANSISTOR MATRIX, published on September 29, 1987;
- 28. Japanese Patent Publication No. 62-120076 to Nasu *et al.*, entitled *THIN FILM TRANSISTOR*, published on June 1, 1987;
- 29. Japanese Patent Publication No. 2000-149766 to Yamada et al., entitled ELECTRON EMISSION ELEMENT AND DISPLAY DEVICE BY USING IT, published on May 30, 2000;
- 30. Japanese Patent Publication No. 11-144709 to Furubayashi *et al.*, entitled *ELECTRODE FOR ELECTROCHEMICAL ELEMENT*, published on May 28, 1999;
- Japanese Patent Publication No. 08-129292 to Arima et al., entitled CHARGE GENERATION CONTROL ELEMENT FOR ELECTROSTATIC IMAGE FORMING DEVICE AND ITS PRODUCTION, published on May 21, 1996; and
- 32. Japanese Patent Publication No. 64-36083 to Arita, entitled AMORPHOUS SILICON

SOLAR CELL, published on February 7, 1989.

Kim et al. '511 relates to a method for forming internetal dielectric of semiconductor device for reducing chemical mechanical polishing process time.

Tanaka *et al.* '157 relates to an active-matrix addressing liquid crystal display (LCD) device having a so-called active-matrix substrate on which pixel electrodes and thin-film transistors (TFTs) are arranged in a matrix array.

Terakado et al. '502 discloses "a liquid crystal display comprising ... a conductive layer formed over said protective layer, said conductive layer including a metallic element; a lower conductive layer provided between said surface and said conductive layer, said lower conductive layer having said metallic element and nitrogen atoms; and an upper conductive layer provided above said conductive layer; said upper conductive layer having said metallic element and nitrogen atoms; wherein said protective layer has a nitrogen concentration of about 10 mol % or more at said surface."

Kubo et al. '096 discloses "forming a film of aluminum sandwiched by films of titanium nitride on said third interlayer insulation film, and patterning said film of aluminum."

Miyazaki et al. '353 discloses "an electronic circuit formed on an insulating substrate and having thin-film transistors (TFTs) comprising semiconductor layers." The thickness of the semiconductor layer is less than 1500 ANG, e.g., between 100 and 750 ANG. A first layer consisting mainly of titanium and nitrogen is formed on the semiconductor layer. A second layer consisting of aluminum is formed on top of the first layer. The first and second layers are patterned into conductive interconnects. The bottom surface of the second layer is substantially totally in intimate contact with the first layer.

Zhou et al. '393 discloses in claim 8 that, "the method of claim 1, wherein said metal layer is a multilayer composed of a titanium/titanium nitride barrier layer and an upper layer of aluminum-copper alloy."

You et al. '630 (Samsung Electronics Co., Ltd.) discloses "the thin film transistor array substrate of claim 1, wherein the intermetallic compound layer is formed of aluminum-molybdenum alloy, aluminum-titanium alloy, aluminum-tantalum alloy, or aluminum0chrome alloy."

Merchant et al. '986 discloses that "a titanium nitride barrier within an integrated contact structure is formed as a multi-layered stack."

Pramanick et al. '625 discloses that "the combination of the titanium nitride layer and the second barrier material provide a superior barrier for conductive material layers, such as, copper/coppre layers, and copper/aluminum layers."

Cuchiaro et al. '927 discloses "a hydrogen diffusion barrier in an integrated circuit is located to inhibit diffusion of hydrogen to a thin film of metal oxide material in an integrated circuit." The hydrogen diffusion barrier comprises at least one of the following nitrides: aluminum titanium nitride (Al.sub.2 Ti.sub.3 N.sub.6), aluminum silicon nitride (Al.sub.2 Si.sub.3 N.sub.6), aluminum niobium nitride (AlNb.sub.3 N.sub.6), aluminum tantalum nitride (AlTa.sub.3 N.sub.6), aluminum copper nitride (Al.sub.2 Cu.sub.3 N.sub.4), tungsten nitride (WN), and copper nitride (CDu.sub.3 N.sub.2).

Matschitsch et al. '965 discloses that "on a silicon semiconductor body an aluminum layer and a diffusion barrier layer that includes titanium are provided." A titanium nitride layer is incorporated into the titanium layer because it has been demonstrated that the titanium nitride layer can compensate for a large proportion of the wafer warping that occurs. Matschitsch '965 also has U.S. Patent No. 6,147,403 that discloses that "on a silicon semiconductor body an aluminum layer

and a diffusion barrier layer that includes titanium are provided."

Leiphart '942 discloses in claim 1 that, "a method of forming an aluminum comprising line having a titanium nitride comprising layer"

Nakamura '572 discloses that "in a semiconductor device such as a thin film transistor ... the protection layer may be formed of titanium or a laminate layer of a titanium layer and a titanium nitride layer."

Hsu et al. '916 discloses in claim 8 that, "the method of claim 7 wherein: the titanium rich titanium nitride layer has a thickness of from about 10 to about 200 angstroms; the substantially stoichiometric titanium nitride layer has a thickness of from about 50 to about 1500 angstroms; and the titanium rich titanium nitride layer promotes adhesion of the substantially stoichiometric titanium nitride layer to the aluminum containing conductor layer."

Harada et al. '026 discloses that "the second aluminum interconnection layer includes a titanium layer, a titanium nitride layer and an aluminum alloy layer."

Inoue '839 discloses that "a titanium nitride barrier layer of 50 to 200 nm in thickness is fabricated between a silicon substrate and an aluminum electrode layer of an IC device."

Parks et al. '296 discloses in claim 1 that, "a process for the fabrication of thin film field effect transistors in active matrix liquid crystal display devices, said process comprising the sequential steps of: disposing a gate metallization layer pattern on a portion of a first major surface of an insulative substrate, said gate metal comprising titanium, said pattern including gate electrodes."

Kuecher et al. '580 discloses that "to improve the planarization and reliability of low-

impedance aluminum metallizations, a substrate provided with a titanium/titanium nitride double layer diffusion barrier layer and having a contact hole is provided or, respectively, filled with an aluminum/silicon alloy sandwich structure composed of a sequence of n aluminum/silicon layers having n-1 intermediate layers of titanium applied thereon, whereby the layer thickness ratio of the titanium intermediate layers to the overall layer thickness d of the metallization behaves like 1:10."

Parks *et al.* '258 discloses in claim 9 that, "the fabrication process of claim 1 in which said source and drain metallization comprises aluminum."

Parks et al. '424 discloses in claim 1 that, "a method for deposition of gate electrode material in an inverted thin film field effect transistor, said method comprising the steps of: disposing a layer of silicon oxide on an insulative substrate; disposing a layer of titanium over said silicon oxide layer; coating said titanium layer with a positive photoresist."

Moeller et al. '756 discloses "solar cells having a semiconductor body composed of amorphous silicon which is deposited on a substrate coated with aluminum at least on one of its surfaces, with a diffusion barrier layer composed of titanium nitride positioned between the aluminum layer and the semiconductor body."

Laska '322 aims at considerably reducing the warpage of semiconductor wafer edges without affecting adherence on the substrate material. English language Abstract is attached.

Ishida '656 relates to the structure and its manufacturing method of the conductive layer formed in the side attachment wall of opening formed in the interlayer insulation film. English language Abstract is attached.

Kawasaki '757 relates to a thin film type thermal head having high reliability by preventing breaking of wire caused by energizing a power feed layer. English language Abstract is attached.

Shankar *et al.* '763 aims at reducing the diffusion of aluminum and silicon between a substrate and a second metallic layer by forming a novel multilayered conductive interconnection layer between the substrate and metallic layer and, at the same time, reducing the formation of spikes or hillocks in an aluminum connection layer. English language Abstract is attached.

Morimitsu *et al.* '464 aims at preventing the variation of pinch-off voltage caused by an usual heat treatment in manufacturing process by forming a gate electrode out of two layers in which highmelting-point metal is used for the first layer of the substrate side and aluminum is used for the second layer. English language Abstract is attached.

Yanai '159 aims at reducing the short-circuit defects of a transistor and obtaining a highly reliable thin film transistor matrix by a method wherein, before formation of a gate insulating film and an operating semiconductor layer, the substrate provided with a gate and a gate bus line, is flattened. English language Abstract is attached.

Nasu '076 aims at decreasing an OFF current, increasing ration of the width to the length of a channel, microminiaturizing it and increasing an allowable current, by increasing the length (channel length) of electron running direction at the end of the channel larger than the center part. English language Abstract is attached.

Yamada et al. '766 aims at emitting electrons stably with a low voltage by forming an insulator layer on an electron supply layer comprising a metal or a metal compound or a semiconductor, and by forming a metal thin film electrode on the insulator layer, and by making the insulator layer and the metal thin film electrode having at least one island region where the film thickness is reduced gradually. English language Abstract is attached.

Furubayashi et al. '709 relates to an electrode for electrochemical element and its

manufacturing method that can efficiently conduct electrons to an inner electroconductive assistant, that can attain a contact with a current collecting part surer and stronger, and that can reduce internal resistance. English language Abstract is attached.

Arima et al. '292 relates to a charge generation control element for electrostatic image forming device with which a drastic reduction of line electrode size and an improvement in dimensional accuracy are made possible and a process for production thereof. English language Abstract is attached.

Arita '083 aims at improving the characteristics of an amorphous silicon solar cell by setting the thickness of a titanium or chrome film in a specific range, thereby effectively utilizing a long-wavelength light. English language Abstract is attached.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

A fee of \$180.00 is incurred by filing of the present information disclosures statement. Applicant's check drawn to the order of Commissioner is attached herewith. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,

Robert E. Bushnell

Reg. No.: 27,774

1522 "K" Street, N.W., Suite 300 Washington, D.C. 20005

Area Code: (202) 408-9040

Folio: P57001 Date: 11/5/04 I.D.: REB/kf

INFORMATION DISCLOSURE STATEMENT

this form with next communication to applicant.

PTO 1A49 (PAGE 1 OF 2)

EMENT	SERIAL NUMBER 10/766564		DOCKET NO. P57001			
	APPLICANT	TAE-SUNG KIM				
:	FILING DATE 29 January 2004		GROUP	2811		

	(A)								
U.S. PATENT DOCUMENTS EXAMINER DOCUMENTS DATE NAME CLASS SUBCLASS ELLING DATE									
EXAMINER	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE			
	6,180,511	1/01	Kim et al.						
	2002/0085157	7/02	Tanaka et al.						
	6,674,502	1/04	Terakado et al.				,		
	6,642,093	11/03	Kubo et al.				-		
	6,608,353	8/03	Miyazaki et al.						
	6,534,393	3/03	Zhou et al.						
	6,518,630	2/03	You et al.						
	6,410,986	6/02	Merchant et al.						
	6,380,625	4/02	Pramanick et al.						
	6,365,927	4/02	Cuchiaro et al.						
	6,309,965	10/01	Matschitsch et al.						
FOREIGN PATENT DOCUMENTS						TRANSLATION			
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO		
	WO 99/08322	2/99	РСТ			Abstract			
	JP09-213656	8/97	Japan			Abstract			
	JP04-265757	9/92	Japan			Abstract			
	JP64-19763	1/89	Japan			Abstract			
	JP59-232464	12/84	Japan			Abstract			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)									
			Γ						
EXAMINER			DATE CONSIDERED:						
EXAMINER:	EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of								

PTO-1449 (PAGE 2 OF 2)			SERIAL NUMBER 10/7665	DOCKET NO. P57001						
			APPLICANT TAE-SUNG KIM							
	STENT S TUR S			FILING DATE 29 January	GROUP	2811				
ATENT DOCUMENTS										
EXAMINER	DOCUMENT NUMBER	DATE		NAME	CLASS	SUBCLASS	FILING DATE			
	6,224,942	5/01	Leiphart							
	6,096,572	8/00	Nakamura	Nakamura						
	5,759,916	6/98	Hsu et al.		_					
	5,341,026	8/94	Harada et al.							
	4,976,839	12/90	Inoue							
	4,933,296	6/90	Parks et al.							
	4,910,580	3/90	Kuecher et al.							
	4,778,258	10/88	Parks et al.							
	4,646,424	3/87	Parks et al.	Parks et al.						
	4,511,756	4/85	Moeller et al.							
FOREIGN PATENT DOCUMENTS TRANSLA							LATION			
	DOCUMENT NUMBER	DATE	C	OUNTRY	CLASS	SUBCLASS	YES	NO		
_	JP62-221159	9/87	Japan				Abstrac	#1 ************************************		
	JP62-120076	6/87	Japan	-			Abstrac	. <u>.</u>		
	JP2000-149766	5/00	Japan				Abstrac			
	JP11-144709	5/99	Japan				Abstrac			
	JP08-129292	5/96	Japan				Abstrac			
	JP64-36083	2/89	Japan				Abstrac			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)										
EXAMINE	<u></u>		DATE CONSIDE	PED:						
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of										
this form with next communication to applicant.										

Approved for use through 9/30/2000. AMB 053-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

	Complete If Known							
FEE TRANSMITTAL	Application Number			er		10/766,564		
Patent fees are subject to annual evision.	Filing Date				2	29 January 2004		
MOV 0 5 2004	Grat Named Inventor			ntor		Tae-Sung KIM		
	Examiner Name				Erdem, F.			
PADEMARK STEEL	Group/Art Unit					2826		
TOTAL AMOUNT OF PAYMENT (\$) 322.00				No.		P57001		
METHOD OF PAYMENT (check one)	Attorney Docket No.				E CALCULATION (c	<i>b</i>		
1. The Commissioner is hereby authorized to charge any	3. /	ADDITIO	NAL FE					
deficiency and credit any over payments to:		Entite	Small	Entitu				
Deposit Account Number:	•	Entity		Entity				
goposk Addodnit Nambor.	Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee D	escription	Fee Paid	
Charge Any Additional Fee Required Under 37 C.F.R. §1.16 and 1.17.	1051	130	2051	65	Surcharge-late filing fee	or oath	\$	
Applicant claims small entity status. See 37 CFR 1.27	1052		2052	25	Surcharge-late provisio	\$		
	1	130	1053	130	Non-English specification	\$		
2. Payment Enclosed:	1812	2,520	1812	2,520	For fling a request for re	eexamination	\$	
(CHECK #48303) ■ Check □ Credit Card □ Money Order □ Other	1804	920*	1804	920*	Requesting publication action	of SIR prior to Examiner	\$	
FEE CALCULATION	1805	1,840 *	1805	1,840*		of SIR after Examiner action	\$	
1. BASIC FILING FEE	1251	110	2251	55	Extension for reply with	n first month	\$	
Large Entity Small Entity	1252	430	2252	215	Extension for reply with	n second month	\$	
Fee Fee Fee Fee	1253	980	2253	490	Extension for reply with	n third month	\$	
Code (\$) Code (\$) Fee Description Fee Paid	1254	1,530	2254	765	Extension for reply with	n fourth month	\$ \$	
1001 790 2001 395 Utility filing fee \$	1255	2,080	2255	1,040		xtension for reply within fifth month		
1002 350 2002 175 Design filing fee \$	1401	340	2401	170	Notice of Appeal			
1003 550 2003 275 Plant filing fee \$	1402	340	2402	170		iling a brief in support of an appeal		
1004 790 2004 395 Reissue filing fee \$	1403	300	2403	150	•	equest for oral hearing		
1005 160 2005 80 Provisional filing fee \$	1451	1,510	1451	1,510	Petition to institute a pu		\$	
SUBTOTAL (1) (\$) .00	1452	110	2452	55	Petition to revive - unav	oidable	\$	
2. EXTRA CLAIM FEES		1,370	2453	685	Petition to revive - uninf		\$	
Extra Fee from Fee Claims below Paid	1501	1,370	2501	685	Utility issue fee (or reiss	sue)	\$	
	1502	490	2502	245	Design issue fee		\$	
Total claims -20** = 3 x \$18.00 = \$54.00 independent -3** = 1 x \$88.00 = \$88.00	1503 1460		2503 1460	320 130	Plant issue fee Petitions to the Commis	ncionar	Φ C	
Independent - 3** = 1 x \$88.00 = \$88.00 Claims	1807		1807	50	Processing fee for prov		\$	
Multiple Dependent =	1806	180	1806	180	-	on Disclosure Statement	\$180.00	
** or number previously paid, if greater; For Reissues, see below	8021	40	8021	40	Recording each patent	assignment per property	_	
Large Entity Small Entity					(Times number of propo	erties)	\$	
Fee Fee Fee Fee Fee Description Code (\$) Code (\$)	1005	160	2005	80	Provisional application	filing fee	\$	
''	1814	110	2814	55	Statutory disclaimer		\$	
1201 88 2201 44 Independent claims in excess of 3	1460	130	laas.		Petitions to the Director		\$.	
1202 18 2202 9 Claims in excess of 20	1801	790	J2801	395	Request for Continued	Examination (RCE)	\$	
1203 300 2203 150 Multiple dependent claim, if not paid 1204 88 2204 44 ** Reissue independent claims over								
original patent 1905 18 2205 9 ** Reissue claims in excess of 20 and	Other	Fee (spe	ecify)				\$	
over original patent	Other Fee (specify) \$						\$	
SUBTOTAL (2) (\$)142.00	** Re	educed	by Ba	asic Fili	ing Fee Paid	SUBTOTAL (3) \$186	0.00	
SUBMITTED BY				Т		lete (if applicable)		
Typed or Printed						· · · · · ·		
Name Robert E. Bushr	ell, E	sq.			Reg. Number	27,774		
Signature Dollar D	ate	5 N	oveml	ber 200		unt		
REB/kf WARNING: Information on this form	may b	ecome	nubli	c. Cred	User ID	should not		